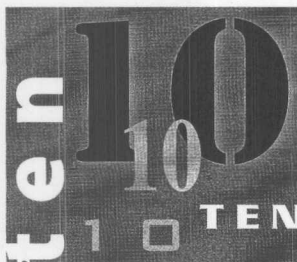# Boundary scan tips optimize test coverage

By Anthony Sparks, technical marketing, JTAG Technologies Inc.

• **To ensure customers** receive high-quality products, engineers must consider testing strategies before they even think about a schematic diagram. These days, most engineers realize boundary scan techniques described in IEEE 1149.1 aptly meet a broad range of test requirements.

But to take full advantage of boundary scan testing, boundary scan must be a required design element and not a nice-to-have add-on. These tips provide design techniques you can use to enhance fault coverage and increase testability of circuits. These techniques save time and work equally as well during prototyping and design testing as they do for production tests.

1 Partition scan chains

Engineers often think—incorrectly—that all boundary scan devices must exist within a single scan chain to participate in one interconnect test. By separating devices into compatible logic families, designers can avoid using level-translation devices.

Today's boundary scan hardware lets developers individually program the output level and input threshold for a test access port (TAP). In some cases, engineers may need to access an individual device to support third-party emulators and debuggers and optimize flash-memory programming. Several boundary scan chains do not decrease test coverage when using an automatic test-pattern generator (ATPG) that supports any number of scan chains and can operate chains individually or in parallel during a single test.

2 Select scanable devices

The success of boundary scan testing depends directly upon the implementation of test structures in ICs. So, when possible, choose devices that already include boundary scan capabilities and consider several things when you select boundary scan devices:

• Has the vendor electrically tested the IC's boundary scan description language (BSDL) file for accuracy and compliance?

A device that does not comply with IEEE 1149.1 can cause test difficulties and may not be available for boundary scan tests, which can drastically reduce anticipated test coverage. The header information in a BSDL file may document verification of syntax, semantics, or electrical characteristics. You also can ask your boundary scan tool vendor if others have used a particular IC successfully in a boundary scan test.

• Does the device support optional boundary scan instructions such as HIGHZ and CLAMP?

These instructions can prove extremely useful in flash-programming applications and some other tests.

• Does the device require compliance patterns, or external logic connections, that let the device operate in boundary scan test mode?

Some boundary scan devices have one or more pins that a circuit must hold in a specified logic state for the device to operate in the 1149.1 mode. In such a case, designers must implement external logic so the proper conditions exist in their circuit during testing. Designers should review BSDL files for COMPLIANCE_PATTERNS that describe these occurrences.
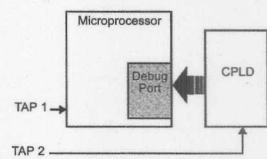

FIG. 1: A CPLD sets up boundary scan test conditions.

3 Ensure devices fully support 1149.1

Some devices, such as DSP ICs and microcontrollers, provide a JTAG TAP for debugging or flash-memory programming, but the TAP does not enable boundary scan testing. In these cases, vendors may refer to devices as IEEE 1149.1 compatible rather than IEEE 1149.1 compliant. The data sheet for a Texas Instruments TMS320C203 DSP IC, for example, notes that although this device has a TAP, it does not have a boundary register so it cannot support boundary scan tests.

Other complications could arise with devices that have multipurpose TAPs. The Freescale MPC860 Processor, for instance, shares its JTAG TAP pins with its background debug mode (BDM) port. When the TAP operates in BDM, these pins do not function as JTAG TAP pins and would break a boundary scan chain for up- or down-stream devices.

In other words, the BDM port is neither compliant nor compatible with IEEE 1149.1. A device could operate in BDM without affecting the TAP pins.

Engineers can exert control over the MPC860's Hard Reset Configuration Word by applying specific values to the data bus during a Hard Reset to force the TAP pins into their JTAG mode. Specifically, bits 11 and 12 must be logic 01 or 11, 00 being the default condition during a hard reset. To ensure these bits get properly set via the MPC860's data bus, use jumpers or a CPLD with a test-purposes-only load as shown in Figure 1.

If you use a complex programmable logic device (CPLD), put it on a boundary scan chain that does not include the MPC860. If both devices exist in the same chain, you cannot program the CPLD while the MPC860 operates in BDM.

4 Bypass noncompliant boundary scan devices

Sometimes you cannot be certain newly released devices or ASICs fully comply with IEEE 1149.1 unless implementation has been verified electrically. In that case, consider placing pads for 0-? resistors, or j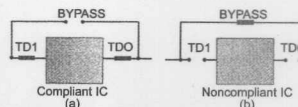umpers, around the device as shown in Figure 2. During test-ing, remove the jumpers before the test data in (TDI) pin and after the test data out (TDO) pin and place a jumper in the bypass position so the scan chain will flow around the device (Figure 2).

5 Take advantage of extra I/O pins

In many designs, FPGAs and CPLDs will have uncommitted I/O pins you can use to produce signals that configure logic circuits or enable test functions. Consider a circuit in which an FPGA and a microprocessor share a data bus with a noncompliant transceiver (Figure 3). If during testing the transceiver's output-enable (OE) signal floats (see red arrow), the transceiver's bus signals could conflict with those produced by the scan chain to test the FPGA-to-processor connections.
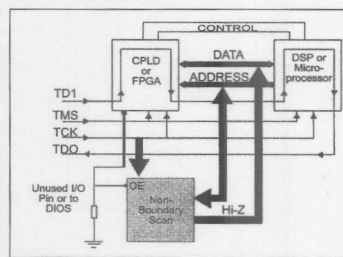

FIG. 3: Unused I/O pin controls non-boundary scan devices.

This type of situation can degrade test coverage. A spare FPGA output or an output from a digital I/O scan (DIOS) module lets you control the transceiver's OE signal and force its outputs into a high-impedance state that does not affect bus tests. And routing this extra trace will not impact the design. When you finally configure the FPGA, define the output as a no-connect so it doesn't interfere with the system's logic circuits (see Tip 7).

6 Control clocks for synchronous devices

Synchronous memories require a clock signal for read or write operations. If engineers do not consider testability during the design process, most likely they will use a simple oscillator, which means boundary scan tests cannot control the clock.

To overcome this limitation, use an uncommitted FPGA output to disable the oscillator and logical-OR the oscillator output with another boundary scan signal to substitute for the system's clock signal. Now, boundary scan tests can control the clock signal and synchronously access the memory.

If this clock drives a clock distribution IC with an internal PLL, it's unlikely a slow boundary scan-generated clock will sync with the PLL. Consequently, the test circuit must bypass it. For example, the IDT MPC9331 PLL Clock Generator IC, for

FIG. 2 a&b: Jumpers bypass noncompliant devices.

Boundary scan tips

example, provides a static bypass path around its PLL so an external clock can control synchronous devices. (FIG. 4) Other clock-distribution ICs provide similar functions.

7 Use flash AutoWrite operations

Traditional applications require a serial bit stream to shift through the entire boundary scan chain once to set up the flash-memory address, data and control lines. Then, the system needs a second shift through the entire chain to toggle the memory's write-enable (WE) to a logic 0 and a third shift to return the WE signal to a logic 1. As a result, a single write operation requires three shifts through the entire chain.

If you can provide external access to the flash-memory WE signal, the controlling boundary scan hardware can toggle it if it supports AutoWrite pulse generation. Then, your circuit only needs a single shift through the boundary scan chain to set up the address, data, and control lines. The boundary scan controller directly toggles the WE signal, which

saves significant time.

Because flash-memory programming often is the most lengthy boundary scan operation, take measures to ensure the shortest programming times. Two major factors determine the efficiency of flash-memory programming via boundary scan techniques: chain length and test-clock (TCK) frequency.

The more devices in a scan chain, the longer it takes to shift bits through the chain. To program flash memories, place boundary scan devices unneeded for programming operations into their BYPASS or, if supported, HIGHZ mode, which reduces their path length to a 1-bit BYPASS register. These registers still form part of the scan chain so you must consider their maximum TCK frequency.

8 Test after configuring FPGAs

Prior to configuration, an FPGA will default to bidirectional I/O lines and preset voltage levels. This situation can cause problems when surrounding circuits require differential signals or specific logic levels. In some cases, damage could occur. Once you configure an FPGA, you can alter its boundary scan capabilities.
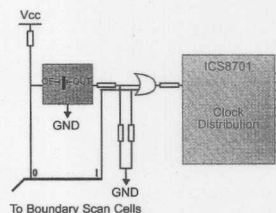

To Boundary Scan Cells

FIG. 4: Extra signals control clock source

Because an FPGA's generic BSDL file reflects preconfigured behavior, you must generate a specific BSDL file based on the FPGA's loaded configuration. Typically, FPGA manufacturers provide software tools that perform this task.

9 Use external modules to test connector lines

During board-level test, connectors on a board may go untested because you lack an external means to drive or sense signals at connector pins. To increase test coverage, add external devices that support boundary scan operations.

Digital I/O modules come in many forms and offer a boundary scan transceiver for each connector pin you must test. These transceivers drive connector pins and capture stimuli generated by boundary scan devices on the board. If you plan to use a

test fixture, digital I/O modules can connect to a board-under-test via test points and spring-loaded probes.

10 Visualize your test coverage

Before you commit to a pcb layout, perform a design-for-testability analysis. Software tools let engineers quickly examine the current potential boundary scan test coverage. Tools also point out areas of the design that lack test coverage and where changes can be made. The Fault Coverage Examiner, for example, can evaluate a design based on BSDL files, net lists for a board, and models of the devices that are not boundary scan compliant.

After engineers identify test gaps, they can determine how to take advantage of unused I/O signals, external digital I/O modules, or different components with boundary scan capabilities. Then, when sufficient boundary scan coverage has been implemented, the pcb is ready for layout.

Conclusion

After you implement as many design-for-test tips as possible, a fault coverage examination can be executed again. The results illustrate the dramatic improvements a few design changes can make in fault coverage.

For more information on boundary scan test techniques from JTAG Technologies Inc., http://ept.hotims.com/20536-112.

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